CLAIMS:

1. A phase locked loop comprising a phase detector for determining a phase difference between a reference signal and mutually phase shifted signals to generate frequency control signals the phase detector comprising: means for obtaining a first one of said frequency control signals by binary multiplication of the reference signal and one of the relative phase shifted signals; and means for obtaining a second one of said frequency control signals by binary multiplication of the relative phase shifted signals.

2. A phase locked loop as claimed in claim 1, further comprising a splitter for generating the relative phase shifted signals the splitter having an input signal generated by a voltage controlled oscillator coupled to the first charge pump and to the low-pass filter.

3. A phase locked loop as claimed in claim 2, wherein the splitter comprises a binary divider receiving a signal generated by the voltage controlled oscillator and generating a binary signal used as a clock signal for a divide by two circuit comprising a first bi-stable circuit ring-coupled to a second bi-stable circuit for generating the relative phase shifted signals.

4. A phase locked loop as claimed in claim 2, wherein the splitter comprises a series coupling of a delay line and an inverter.

5. A phase locked loop as claimed in claim 2, wherein the voltage controlled oscillator is a quadrature oscillator generating signals that are in quadrature to each other, the relative phase shifted signals being in quadrature.

6. A phase locked loop as claimed in claim 1, further comprising a frequency detector coupled to receive the reference signal and the relative phase shifted signals for supplying an up frequency detector signal) and a down frequency detector signal to a first charge pump coupled to the loop filter.

7. A phase locked loop as claimed in claim 6, wherein the frequency detector comprises a third flip-flop and a fourth flip-flop driven by the reference signal and having at their inputs the relative phase shifted signals, outputs of the flip-flops being coupled to input terminals of a fifth flip-flop the phase detector generating the up frequency detector signal obtained by binary multiplication between a signal generated by the fifth flip-flop at it's output and the signal obtained at the bar-output of the fourth flip-flop, and further generating the down frequency detector signal obtained by binary multiplication of the signal obtained at a bar-output of the fourth flip-flop and the signal obtained at a bar-output of the fifth flip-flop signal obtained at the bar-output of the fourth flip-flop.